Part Number	Package	Marking
HGP130N12SL	TO-220	

Parameter	Symbol		Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25℃	71	
			120	V
				V
			260	A

	Symbol
Thermal Resistance Junction-Case	

Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250 A	120	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250 A	1.4	2.0	2.4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=120V, T_j=25℃	-	-	1	A
		V_{GS}=0V, V_{DS}=120V, T_j=100℃	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	9.8	12.5	m
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=4.5V, I_D=20A	-	12	17	m
Transconductance	g_{fs}	V_{DS}=5V, I_D=20A	-	65	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	2.2	-	

Dynamic Characteristics

Parameter	Symbol	Conditions	min	typ	max	Unit
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=60V, f=1MHz	-	2056	-	pF
Output Capacitance	C_{oss}		-	222	-	
Reverse Transfer Capacitance	C_{rss}		-	7.9	-	
Total Gate Charge	Q_g(10V)	V_{DD}=60V, I_D=20A, V_{GS}=10V	-	31	-	nC
Total Gate Charge	Q_g(4.5V)		-	15	-	
Gate to Source Charge	Q_{gs}		-	8	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	4	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=60V, I_D=20A, V_{GS}=10V, R_G=10 ,	-	11	-	ns
Rise time	t_r		-	9	-	
Turn off Delay Time	$t_{d(off)}$		-	18	-	
Fall Time	t_f		-	10	-	

Reverse Diode Characteristics

Parameter	Symbol	Conditions	min	typ	max	Unit
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=60V, I_F=20A, dI_F/dt=100A/ s	-	50	-	ns
Reverse Recovery Charge	Q_{rr}		-	75	-	nC

Fig 1. Typical Output Characteristics

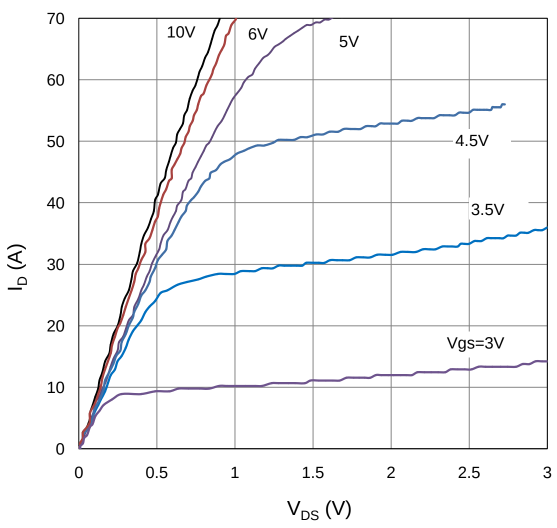


Figure 2. On-Resistance vs. Gate-Source Voltage

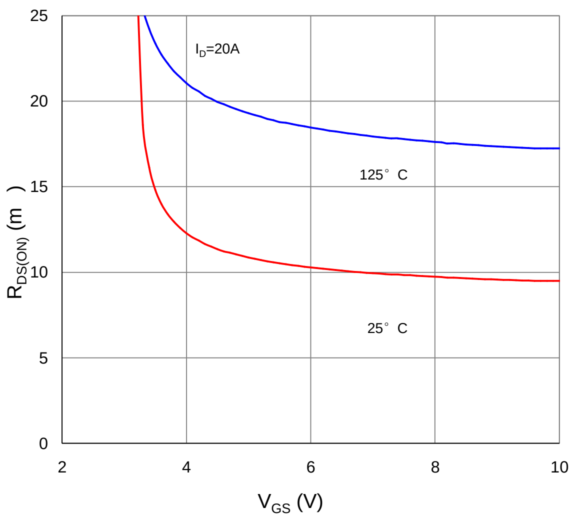


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

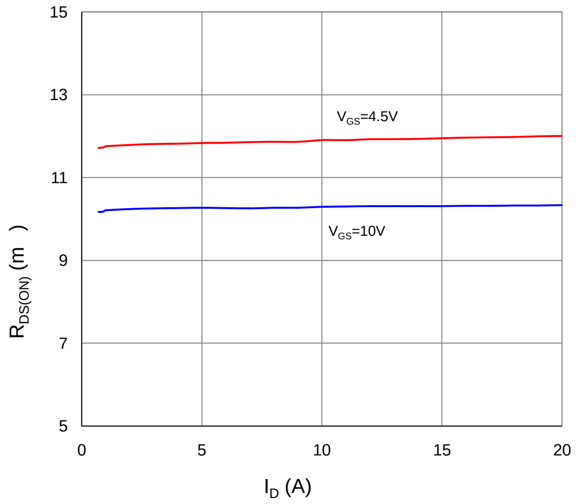


Figure 4. Normalized On-Resistance vs. Junction Temperature

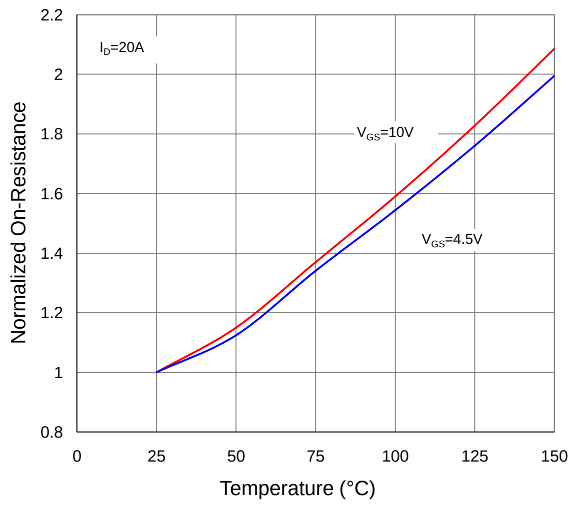


Figure 5. Typical Transfer Characteristics

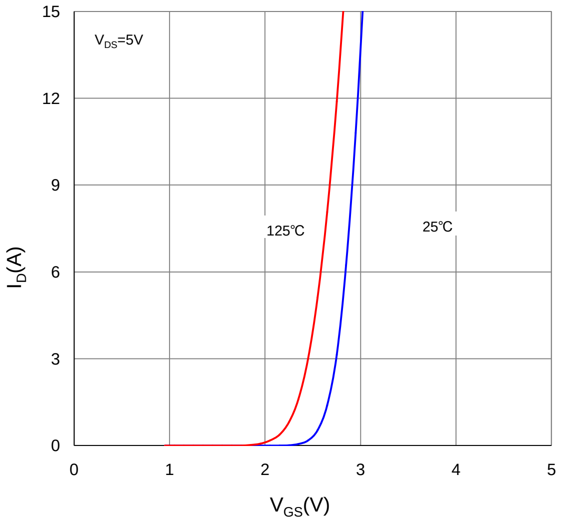


Figure 6. Typical Source-Drain Diode Forward Voltage

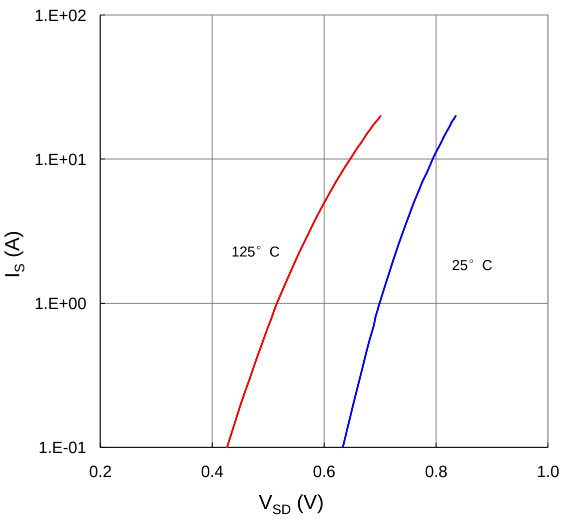


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

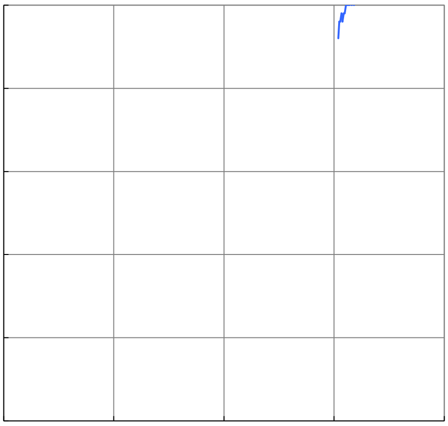


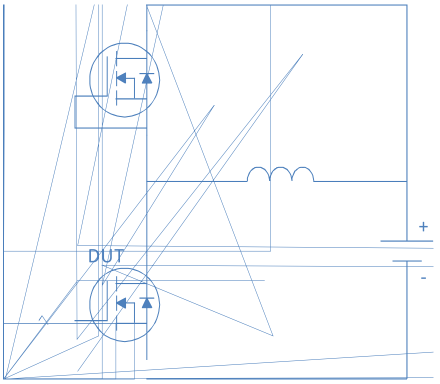
Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

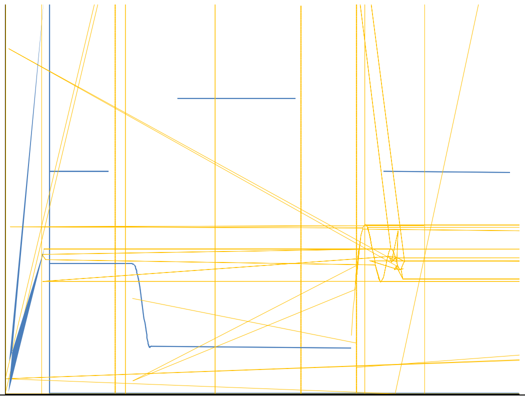
Figure 9. Maximum Safe Operating Area

Figure 10. Maximun Drain Current vs. Case Temperature

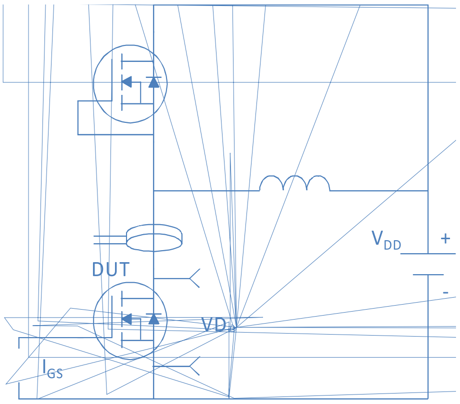
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

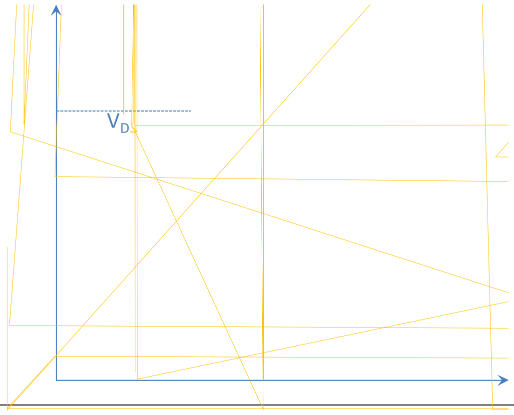
Inductive switching Test



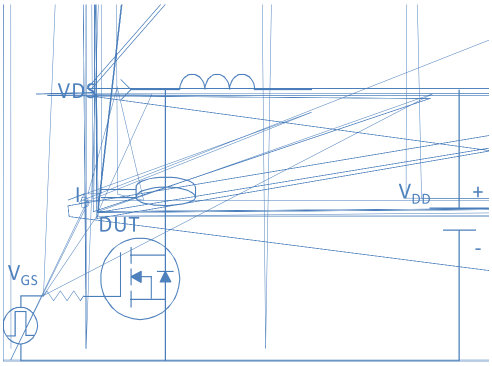


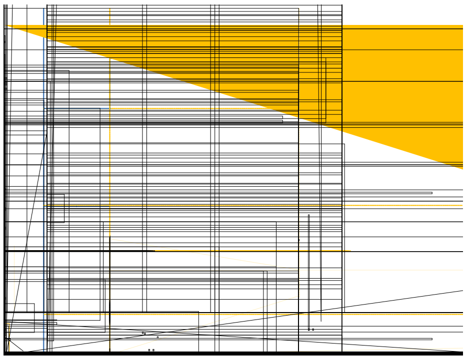
Gate Charge Test



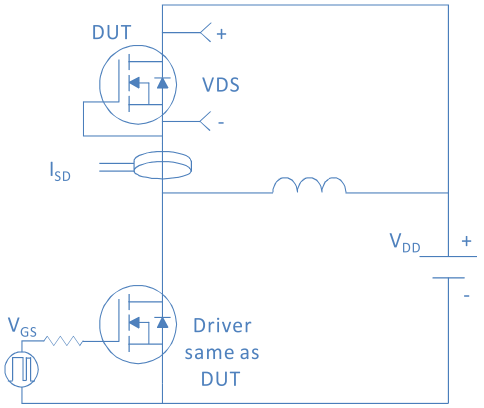


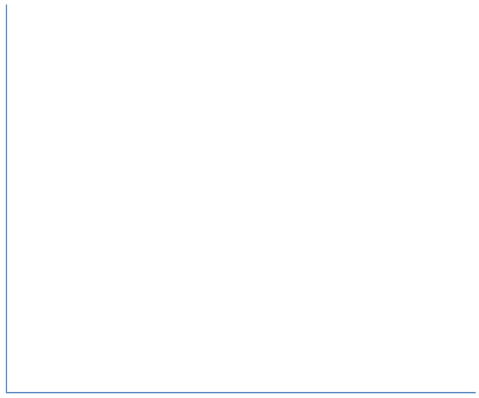
Uclamped Inductive Switching (UIS) Test





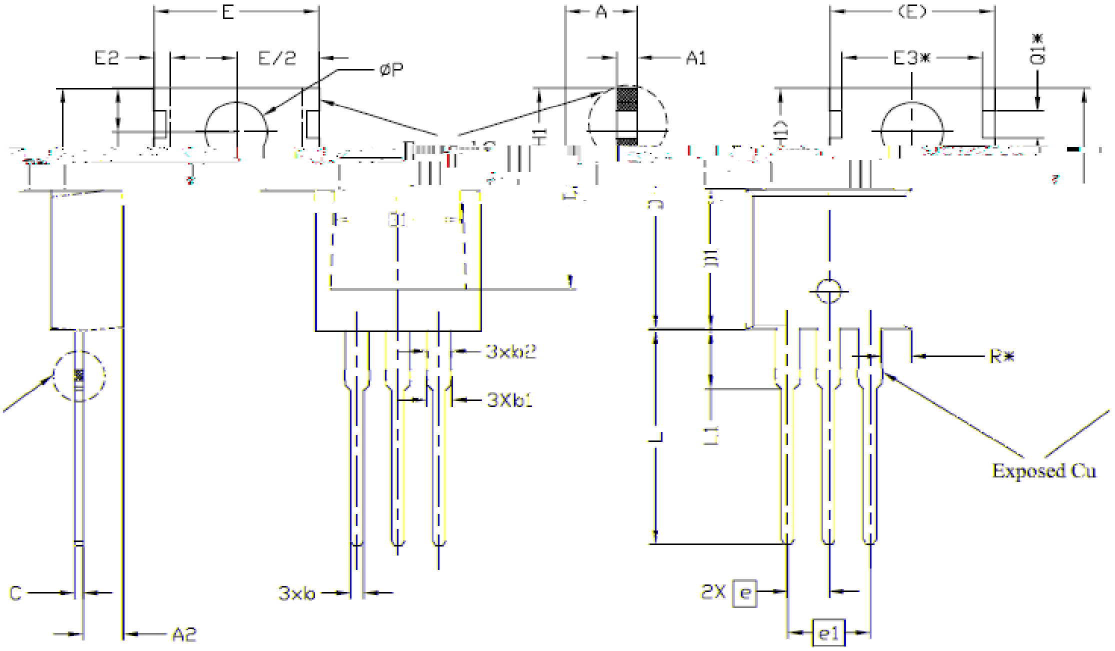
Diode Recovery Test





Package Outline

TO-220, 3 Leads



SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	[illegible]	[illegible]	[illegible]	
A1	[illegible]	[illegible]	[illegible]	
A2	[illegible]	[illegible]	[illegible]	
b	[illegible]	[illegible]	[illegible]	
b1	[illegible]	[illegible]	[illegible]	
b2	[illegible]	[illegible]	[illegible]	
c	[illegible]	[illegible]	[illegible]	
D	14.70	[illegible]	16.00	4
D1	[illegible]	[illegible]	9.02	
D2	12.83	[illegible]	[illegible]	[illegible]
E	9.92	10.12	10.32	4,5
E1	[illegible]	[illegible]	[illegible]	[illegible]
E2			[illegible]	[illegible]
E3*		[illegible]		
e		2.54BSC		
e1		5.08BSC		
H1	[illegible]	6.45	[illegible]	[illegible]
L	13.47	13.72	13.97	
L1	[illegible]	[illegible]	4.00	
ØP	[illegible]	[illegible]	[illegible]	
Q	[illegible]	[illegible]	[illegible]	
Q1*		1.72REF		
R*		[illegible]		